AMENDMENT TO THE CLAIMS

This listing of claims will replace all prior versions of claims in the application.

Listing of Claims:

1. (currently amended) An electrostatic discharge (ESD) protection circuit for an integrated circuit, the ESD protection circuit comprises:

ESD clamping circuit operably coupled to a first power pin of the integrated circuit and a second power pin of the integrated circuit;

ESD triggering circuit operably coupled to the ESD clamping circuit, wherein, when enabled and when sensing an ESD event, the ESD triggering circuit provides a clamping signal to the ESD clamping circuit such that the ESD clamping circuit provides a low impedance path between the first and second power pins, the ESD triggering circuit having a first time response to sense the ESD event and a second time response for the clamping signal to activate the ESD clamping circuit, in which the first time response is different than the second time response; and

ESD disabling circuit operably coupled to disable the ESD triggering circuit when the integrated circuit is in a normal operating mode, wherein the ESD disabling circuit includes an N-channel transistor, in which the source of the N-channel transistor is coupled to ground of the integrated circuit and the drain of the N-channel transistor is coupled to disable the ESD protection circuit when the N-channel transistor is on, and wherein the ESD disabling circuit further includes a delay module operably coupled to enable the N-channel transistor after a delayed sensing of an ESD disable signal.

2. (original) The ESD protection circuit of claim 1, wherein the ESD clamping circuit comprises at least one of: a transistor, a surge suppressor, and a silicon controlled rectifier.